MICROMACHINED LOW DISPERSION INTERCONNECTS FOR OPTOELECTRONIC ARRAY PACKAGING

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Abstract — **A micromachined microstrip interconnect, partially shielded on the top surface, is designed, fabricated, and measured for use in optical array packaging applications. Field simulations show the interconnects to be highly isolated for an array pitch of 500 μm. S-parameter, relative phase constant, and attenuation curves are shown up to 40 GHz for 1 cm long 50-ohm designs. The structure exhibits 1.4 dB/cm of attenuation at 40 GHz and a phase constant that has only ± 0.5% variation across the band. The micromachined partially shielded microstrip offers high isolation, low dispersion, and low attenuation that is necessary for arrayed interconnects.**

I. INTRODUCTION

The combined design of high-speed data communications with telecommunications technology requires new design methods for integrating high-speed RFIC designs, used for electronic drive circuits, with high data rate optoelectronic components. In response to this shift, there is a significant need to develop advanced packaging methods that are complementary to chip-level electronic and photonic packaging. Two examples include vertical cavity surface emitting laser (VCSEL) high density arrays that are operated in parallel [1] and optical modulators being considered for 10+ Gbps and 40+ Gbps applications, respectively. While optical design scaling is used to produce high performance laboratory devices, an important issue ultimately impacting the deployment of such circuits is the disappointing performance differences observed between pre- and post-packaged devices.

The role of the photonic package has been aimed at addressing three main issues: (1) precision alignment and placement, (2) thermal management, and (3) low cost manufacturing methods. In miniature system design, the use of silicon optical microbench technology has been used to address many of these issues and has provided an important solution to chip level packaging for photonic applications. To date, significant benefits have already been realized for hybrid integration of optical fiber to laser diodes and alignment of discrete components used in low and medium data rate applications. Unfortunately, for high data rate applications, which require GHz electronic interfaces, a fourth issue must now be added to the design criteria: low electromagnetic interference effects.

Modulation at RF frequencies can make a design sensitive to unwanted parasitic effects introduced by the package as well as to electromagnetic coupling between nearby electronic interconnects. Both these issues can have a substantial impact on the performance of a packaged optical device. Furthermore, package diagnostics generally require complete system assembly (a time intensive process) before data can be obtained regarding performance and/or assessment and execution of redesign priorities; a process that can be difficult to implement in a timely and cost effective manner.

This article reports the investigation of novel interconnect designs for use in optoelectronic packaging applications that offer low dispersion for wide bandwidths (i.e. 40 GHz) and is capable of low cross coupling between adjacent signal lines. The approach is compatible with silicon optical microbench technology and has the potential to produce a paradigm shift in evaluation of photonic package designs from a backend system process to a middle or front-end process. In this work, we present the design and characterization of micromachined microstrip and coplanar waveguide interconnect. These designs provide 50-ohm impedance matching between RF source and the optical devices as well as spatially consistent dimensions needed for closely spaced laser devices used in VCSEL array applications. Finally, the approach offers important on-wafer test capability to a silicon optical microbench design with integrated interconnects for preliminary package diagnostic testing of electronic parasitics and coupling at RF frequencies.

II. DESIGN AND FABRICATION APPROACH

A. Design of micromachined partially shielded microstrip

A micromachined partially shielded microstrip (PSM) design combines both the low dispersion of a coplanar waveguide (CPW) with isolation in a microstrip design. Comparison structures consist of a reduced and full substrate height coplanar waveguide design that can also

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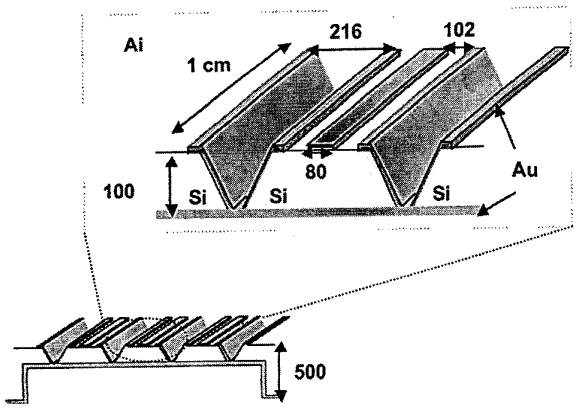

Fig. 1 Partially shielded microstrip in an array configuration and as a single transmission line. All dimensions are in microns unless otherwise denoted.

be incorporated into the partially shielded configuration.

Typical VCSEL die array configurations have a pitch of 250 microns. In this study, 500 micron pitch spacing has been used to demonstrate the concept although 250 micron pitch designs are possible. To minimize conductor loss effects, an interconnect width (W) of 80 μm is chosen for CPW and microstrip designs. In the initial CPW design, the gaps (G) and ground plane (W_G) have widths of 47 μm and 78 μm, respectively, and are chosen to provide a 50 Ω characteristic impedance (Z_o). In the microstrip design, the top conductor is surrounded by ground electrodes that are incorporated on the upper surface to offer partial shielding on the top surface of the design and signal ground equalization. The placement and dimensions of the electrodes are chosen to support a 50 Ω microstrip mode with dimensions for G of 102 μm and W_G of 216 μm, respectively, for a 50 Ω characteristic impedance (Fig. 1). The total ground conductor width traversing the top surface and groove is 322 μm.

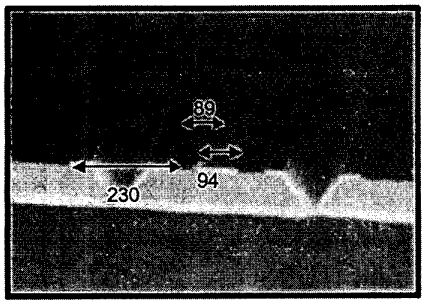

Fig. 2 SEM image of partially side shielded microstrip. All dimensions are in microns.

For the partially shielded microstrip, the fabricated dimensions W-G-W_G are 94-89-230 microns. The result is a 43 Ω characteristic impedance line. Since both CPW and PSM lines are fabricated together, the resulting CPW dimensions W-G-W_G are 85-39-88 microns producing a Z_o of 44 Ω. The final fabricated dimensions differ due to diffraction and current crowding from the nonplanar electroplated photoresist technique used for circuit formation [2] (See Section II. B. for details). These discrepancies will be compensated for in future mask designs. The Scanning Electron Microscope (SEM) image in Fig. 2 shows the final dimensions of a sample PSM line.

Applied to an array, the design shown in Fig. 3 has a pitch of 500 microns, which would connect to every other VCSEL on a typical die. This choice, allows relaxed tolerances for the initial development of the topside metallized grooves. Field simulations show that the partially shielded microstrip will be highly isolated and dominated by the microstrip mode. An array of PSM's is shown in Fig. 3, where the field strength direction is primarily toward the ground plane.

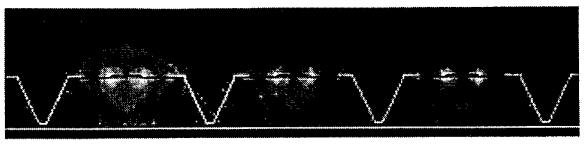

Fig. 3 Field simulation of shielded microstrip design (light=high intensity field, dark=low intensity field)

B. Fabrication of partially shielded microstrip lines

The full and reduced height CPW lines are developed using standard silicon IC and micromachining technologies similar to [3]. The partially shielded microstrips incorporate nonplanar fabrication techniques as well to develop the circuits. A 500 μm double-side polished, high resistivity silicon wafer (>2000 ohm-cm with (100) orientation) is used as the substrate. Nitride films (900 Å) are removed prior to printing circuits. The circuits lie only on silicon and are formed by evaporating Ti (400 Å)-Au (2000 Å) as a seed layer for electroplating.

In Fig. 4(a), the nitride film is patterned with dry (RIE) etching and is used to mask the silicon in a KOH wet-etch. The KOH anisotropically etches silicon to produce the angled profile shown in Fig. 4(a). This etch forms the topside grooves. Traditional spin-coated photoresist (PR) applies unevenly over a nonplanar surface and results in poor photolithography; therefore, a negative conformal photoresist (Shipley Eagle 2100) is electroplated using an evaporated Ti/Au seed layer as a metal cathode. Shipley Eagle 2100 PR is an aqueous photoresist with a 10% solid

(micelle) concentration. The micelles become positively charged and migrate in an electric field to the cathode [2]. A four-inch aluminum plate is used as the anode. The resist is found to plate thicker in the inner corners due to current crowding, and slight overdeveloping is used to compensate for the thicker plating. The resultant undercut causes an increase in

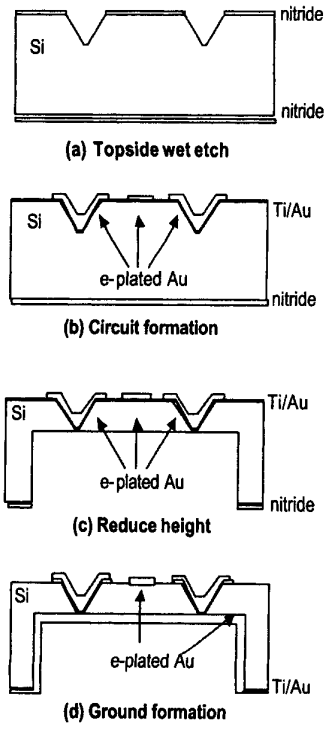

Fig. 4 Microfabrication design process for a single partially shielded microstrip.

conductor dimensions and a decrease in the gap [2]. In Fig. 4(b), four micron thick gold conductors are formed by electroplating to the Ti/Au seed layer using the electroplated photoresist as a mold. Fig. 4(c) and (d) provide the backside processing needed to reduce the substrate heights and complete the metallization. The bottom is dry plasma etched to 390 μm and the remaining 10 μm is etched in the KOH bath to ensure uniform contact with the gold on the front sides. To complete the process, a Ti-Au seed layer is sputtered onto the backside and four microns of gold are electroplated to form the lower ground plane. The SEM image in Fig. 2 shows a cross section of the partially shielded microstrip line on reduced-thickness substrate.

III. DISCUSSION AND RESULTS

A. Measurement Setup

Two-port S-parameters are obtained using Cascade Microtech 150 micron pitch, air-coplanar probes and on-wafer station. All test structures include a 250 μm feedline such that a through-reflect-load (TRL) calibration can be done. A through, open, and three delay lines lengths of 900, 2600, and 7800 microns are used to calibrate for a bandwidth of 40 GHz. The reference plane at the inputs to the device under test (DUT) is established using the calibration standards located on the same silicon substrate and is processed using the NIST algorithm, Multi-Cal: DEEMBED [4]. All DUT lengths are 1 cm long between the TRL reference planes.

B. Simulation and Experimental Results

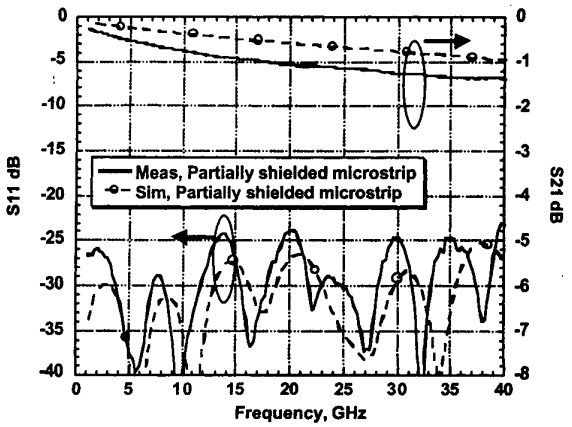

Fig. 5 Magnitude S_{11} and S_{21} for partially shielded microstrip line both fabricated and HFSS simulation.

The substrate parameters used in both simulation and fabrication are based on ε_r of 11.7, tanδ of 0.003, and a gold conductor thickness of 4 μm. The PSM return loss and transmission loss data is compared to full-wave solver simulation (HFSS [5] and Maxwell 2D Extractor [6]) in Fig. 5. The return loss is consistently below -23 dB across the band and the insertion loss is -1.4 dB at 40 GHz. HFSS and Maxwell 2D Extractor both calculate a characteristic impedance of 43 Ω across the band for the fabricated dimensions. Ansoft's HFSS S-parameter data shows slightly lower insertion loss at 40 GHz of 1 dB/than the measured values. The simulation does not account for slight variations in the etch depth of the deep bottom side dry plasma etch of 400 μm, variations in gold plating depth due to current variations in the nonplanar geometry, or the known reduction in resistivity that occurs from high

temperature process (~1000 °C) used to deposit the nitride film.

The PSM is compared to a 44 Ω reduced height and full height CPW lines in Fig. 6 and 7. As expected for CPW, the phase constant is flat across the band, which indicates low distortion. The PSM also exhibits this property with only a ± 0.5% deviation across 40 GHz, which is excellent for wideband high speed interconnect performance. The higher phase constant of the PSM is a result of the microstrip mode causing more fields to be contained within the substrate, thus a higher effective dielectric constant. The lower attenuation of the PSM is also more indicative of a microstrip mode structure (Fig. 7).

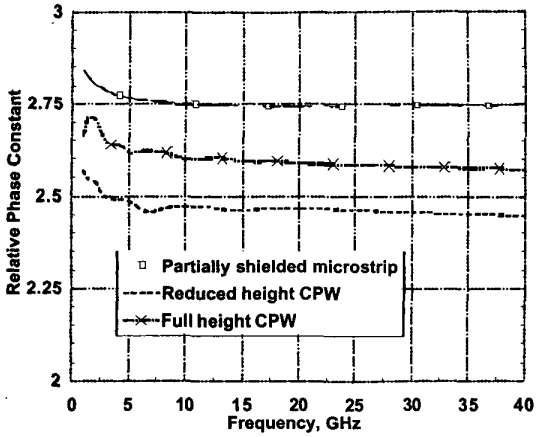

Fig. 6 Measured relative phase constant for partially shielded microstrip compared with reduced height CPW and full height CPW.

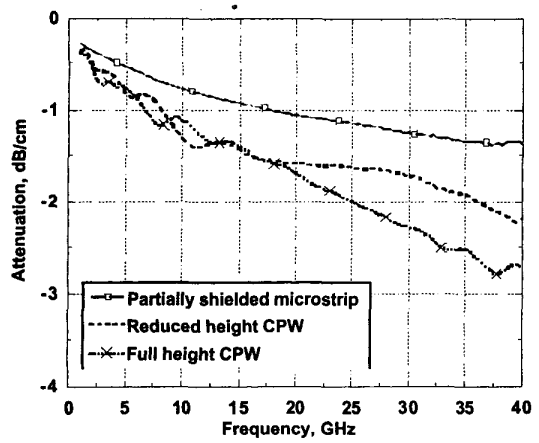

Fig. 7 Measured attenuation for partially shielded microstrip compared with reduced height CPW and full height CPW.

When compared to a reduced height 50 Ω microstrip of similar dimensions (W=80 μm, h=100 μm) [3], the return loss and insertion loss are similar. The attenuation in the reduced height microstrip is 1.7 dB/cm at 40 GHz, with oscillations beginning at 25 GHz. The PSM has a strongly linear attenuation of 1.4 dB/cm up to 40 GHz. The PSM also has a nearly flat phase constant, which indicates lower distortion across the band. These properties make the PSM an optimum interconnect for array packaging and offer the advantages the low attenuation of a microstrip and the low distortion of CPW.

IV. CONCLUSION

A micromachined partially shielded microstrip was fabricated using nonplanar photolithography techniques. The resulting structure exhibits lower attenuation than CPW designs of the similar dimensions and only ± 0.5% deviation in the phase constant across the band. Hence, partially shielded microstrips offer low distortion and losses as well as the high isolation required for high-speed array packages.

ACKNOWLEDGEMENT

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